CLAIM AMENDMENTS

This listing of claims will replace all prior versions and listings of claims.

1. (Currently Amended) A method of determining a maximum ~~optimum~~ clock frequency ~~at which a~~ of an operation of a digital processing system ~~can operate~~, the method comprising ~~the steps of~~:

generating a clock signal at an initial frequency;

increasing said initial frequency in a step-wise manner; ~~and~~

determining the operation of said digital processing system at each of a selected number of frequencies with a timing monitor, until a clock frequency is identified at which said digital processing system does not operate correctly within system timing constraints; ~~and~~

identifying ~~a~~ the maximum clock frequency ~~at which~~ of the operation of said digital processing system ~~can operate correctly~~; and

using the maximum clock frequency only during a run time when the digital processing system is starving output signals and blocking input signals,

wherein ~~characterized in that:~~ said maximum clock frequency comprises ~~the~~ a frequency immediately previous to the ~~one~~ clock frequency

identified as ~~being one~~ the clock frequency at which said digital processing system does not operate correctly~~; and in that~~

~~a timing monitor is provided for determining whether or not said processing system can operate within system timing constraints at each frequency, thereby indicating whether or not said system operates correctly at the respective frequency, said timing monitor monitoring at least a level of input and output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system~~.

2. (Currently Amended) ~~A method according to~~ The method of claim 1, further comprising: ~~including the step of~~

storing the maximum frequency in a ~~memory~~ programmable delay element.

3. (Currently Amended) ~~Method of calibrating clock generation means in a digital processing system~~The method of claim 1, further comprising:

periodically performing the method of claim 1 ~~while the system is running~~ during the run time

~~, and applying the resultant maximum frequency to said clock generation means~~.

4. (Currently Amended) ~~Apparatus for determining~~ An apparatus that determines a maximum ~~optimum~~ clock frequency ~~at which~~ of an operation of a digital processing system ~~can operate~~, the apparatus comprising:

~~means for generating~~

a programmable ring oscillator that generates a clock signal at an initial frequency;

a frequency finder and selector that increases the frequency of the clock signal from the initial frequency to the maximum clock frequency ~~means for increasing said frequency~~ in a step-wise manner;

~~and means for~~

a timing monitor that determines ~~determining~~ the operation of said digital processing system at each of a selected number of frequencies, until a clock frequency is identified at which said ~~processor~~ digital processing system does not operate ~~correctly;~~ correctly within system timing constraints, ~~and~~ thereby

~~means for~~ identifying ~~a~~ the maximum clock frequency at which said digital processing system can operate correctly;

wherein the maximum clock frequency is used only during a run time when the digital processing system is starving output signals and blocking input signals, and

~~characterized in that:~~

wherein said maximum clock frequency comprises ~~the~~ a frequency immediately previous to the ~~one~~ clock frequency identified as ~~being one~~ the clock frequency at which said digital processing system does not operate correctly~~; and in that~~

~~said means for determining the operation of said system comprises a timing monitor for determining whether or not said system can operate within system timing constraints at each frequency, thereby indicating whether or not said system operates correctly at the respective frequency, by monitoring at least a level of input and output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system~~.

5. (Currently Amended) A method of selectively changing the frequency at which a digital processing system is operating, the method comprising:

~~a)~~ determining, when said digital processing system is reset, a maximum clock frequency at which said digital processing system can operate within system timing constraints;

~~, determining by maintaining a level of input and output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system and~~

storing said maximum frequency;

~~b)~~ generating, after reset, a clock signal at a nominal frequency, less than said maximum frequency, until a signal is received indicating that an increased clock frequency is required;

~~c)~~ generating, in response to receipt of said signal, a clock signal at said maximum frequency ~~for a required time~~ only during a run time when the digital processing system is starving output signals

~~; and then d) once again generating a clock frequency at said nominal frequency~~.

6. (Currently Amended) ~~A method according to~~ The method of claim 5, ~~wherein the step of determining said maximum frequency comprises~~ further comprising;

using a bi-section algorithm when determining the maximum clock frequency

~~generating a clock signal at an initial frequency;~~

~~increasing said frequency in a step-wise manner and determining the operation of said system each of a selected number of frequencies, until a clock frequency is identified at which said processing system does not operate correctly; and~~

~~identifying a maximum clock frequency at which said system can operate correctly; characterized in that:~~

~~said maximum clock frequency comprises the frequency immediately previous to the one identified as being one at which said system does not operate correctly; and in that~~

~~a timing monitor is provided for determining whether or not said processing system can operate within system timing constraints at each frequency, thereby indicating whether or not said system operates correctly at the respective frequency, said timing monitor monitoring at least a level of input and output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system~~.

7. (Currently Amended) ~~Apparatus for selectively changing~~ An apparatus that selectively changes the frequency at which a digital processing system is operating, the apparatus comprising:

~~i. a~~ a programmable ~~clock generation means~~ ring oscillator that only generates a maximum clock frequency;

an external source that generates a nominal clock frequency;

~~ii. means for determining~~ a timing monitor that determines, when said digital processing system is reset, ~~a~~ the maximum clock frequency at which said digital processing system can operate within system timing constraints;

a frequency finder that detects the maximum clock frequency of the programmable ring oscillator; and

a clock multiplexer that switches between the nominal clock frequency and the maximum clock frequency, using the maximum clock frequency only during a run time when the digital processing system is starving output signals and blocking input signals

~~determining by maintaining a level of input and output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system and storing said maximum frequency, and storing said maximum frequency; and iii. means for causing said clock generation means to: a) generate, after reset, a clock signal at a nominal frequency, less than said maximum frequency, until a signal is received indicating that an increased clock frequency is required; b) generate, in response to receipt of said signal, a clock signal at said maximum frequency for a required time; and then c) once again generate a clock frequency at said nominal frequency~~.

8-14. (Canceled).